Impact of Current Flow Diverter on Innovative HTS Tape Architectures for DC Fault Current Limitation at Electric Fields up to 150 V/m

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***Abstract*—In this work, we use numerical simulations to compare the performance of different promising architectures of HTS tape for DC fault current limitation. A 1-D finite-element model which solves the heat equation through the thickness of a high-temperature superconducting (HTS) tape at the location of a hot spot was coupled with a simple electrical circuit model to perform the simulations. Using the normal zone propagation velocity (NZPV) obtained from a distinct 3-D finite-element electrothermal model, the quench dynamics in HTS tapes can be predicted, which allows estimating quite accurately the fault current level vs time. The calculations indicate that the insertion of a current flow diverter in the tape architecture allows decreasing the fault current level more rapidly and reducing the temperature elevation, thanks to the increased NZPV.**

***Index Terms*—Fault current limiters, high temperature superconductors, high voltage direct current transmission systems, finite element analysis, hot spots.**

I. Introduction

SUPERCONDUCTING fault current limiters (SFCLs) are considered as one of the most promising applications of high temperature superconducting (HTS) tapes. While actual commercial HTS tapes have been used in many medium voltage SFCLs (between 12 and 25 kV) and even in some high voltage SFCL prototypes, there is still a need to increase the electric field that REBCO tapes can withstand during fault current limitation in order to implement more compact and more cost-effective SFCLs. This is particularly important in order to reduce the footprint of this equipment in a power substation. The H2020 European project FASTGRID aims at developing the best conductor design that fulfill these requirements [1], with a specific focus on SFCLs for HVDC grids. More specifically, the FASTGRID project targets conductors able to withstand up to 150 V/m during 50 ms. The final objective is to demonstrate the use of these tapes in a 50 kV DC demonstration module.

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In order to ensure the reliability of a SFCL device, the HTS tape must first withstand a clear fault. In the present case, this corresponds to applying an electric field of 150 V/m for 50 ms. In order to limit the temperature elevation in the tape during a clear fault, the tape must possess a sufficient thermal mass, which is generally obtained by adding a thick shunt [2].

Another scenario to be considered is the development of a hot spot [3]. At present time, commercial HTS tapes possess a local critical current I_c that vary along their length (approximately $+/-20\%$ of variation). This variation is inherent to the fabrication process. In the case of a prospective fault current that corresponds to the minimum value of the local I_c of the tape, only a small zone will quench (called hot spot). Considering the low normal zone propagation velocity (NZPV) of commercial HTS tapes, a local destruction of the tape at the hot spot location thus becomes very likely [4], [5]. Besides increasing the homogeneity of I_c by improving the fabrication process, another solution to mitigate the hot spot issue is to add a conductive shunt in order to reduce the Joule losses [2], [6].

Another solution is to homogenize the quench by increasing the NZPV of HTS tapes [7]. A promising way to increase the NZPV is the current flow diverter (CFD) concept [8]–[10]. In the CFD concept, a highly resistive layer that partially covers the HTS-Ag interface is added, which forces the current to flow through the edges of the HTS tape.

Alternately, the use of a sapphire substrate instead of a Hastelloy substrate is attractive because it possesses a much higher thermal conductivity at cryogenic temperatures. Therefore, it dissipates more efficiently the local heat generated in a quenched zone. Furthermore, a higher NZPV was observed on YBCO films grown on a sapphire substrate as compared to films grown on Hastelloy substrates [11], [12].

In this work, we compare the quench behavior of promising tape architectures using numerical simulations. The quench behavior in DC limitation was simulated with a 1-D model implemented in COMSOL, a commercial finite-element software. A distinct 3D electrothermal model was used to obtain the NZPV of the tape architectures investigated.

II. 1-D Electrothermal Model

A 1-D electrothermal model was used to calculate the current and the temperature in a HTS tape at the location of a hot

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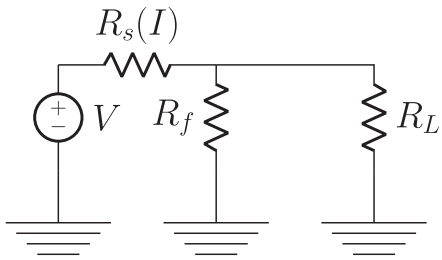

Fig. 1. Electrical circuit used to simulate a fault current in a DC system.

spot. The dimension simulated corresponds to the thickness of the HTS tape. At the beginning of the simulation, the model assumes that the HTS has quenched at the hot spot(s) location(s). Finite-element simulations are performed using the heat transfer module of the COMSOL Multiphysics 4.3b software package. The variable solved for is the temperature T, which is calculated using the heat equation:

$$\rho_m C_p(T)\frac{\partial T}{\partial t} + \nabla \cdot (-k(T)\nabla T) = Q_j, \tag{1}$$

where ρ_m is the mass density, $C_p(T)$ is the heat capacity, $k(T)$ is the thermal conductivity and Q_j represents the Joule losses, i.e.:

$$Q_j = \rho(T) J^2. \tag{2}$$

We assume no heat exchange between the HTS tape and its surrounding (adiabatic conditions). The following Neumann boundary condition is thus applied on both surfaces of the tape:

$$\mathbf{n} \cdot \nabla T = 0. \tag{3}$$

The electrical behavior of the DC circuit is approximated by a voltage source connected in series with two resistances. The first resistance R_s represents the SFCL: its value depends on the current flowing in the SFCL. The second resistance R_L represents the equivalent load of the DC circuit in normal conditions, i.e. no fault (see Figure 1). The SFCL is placed directly after the voltage source, assuming that the line resistance is negligible. This corresponds to the worst scenario for a SFCL, since the entire source voltage is seen at the SFCL terminals in case of clear fault. To simulate a fault current, a resistance R_f is placed in parallel with R_L. The value of R_f is adjusted in order to control the level of the prospective fault current. The total resistance seen by the DC source R_{tot} is thus given by

$$R_{tot} = R_s + \frac{R_L R_f}{R_L + R_f}. \tag{4}$$

The total length of the tape corresponds to NL_d, where N is the number of simultaneous hot spots and L_d is the distance between each hot spot. We assume that the hot spots are equally distant (see Figure 2), which statistically speaking, would correspond to the mean distance between each hot spot. The total length of the tape is fixed by the voltage of the electrical circuit V and the maximum electric field E_{max} that the HTS tape must be able to withstand, i.e.

$$V = E_{max} N L_d. \tag{5}$$

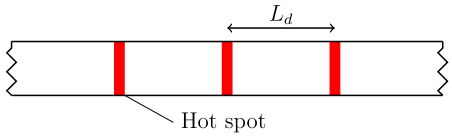

Fig. 2. The model assumes that the distance between the hot spots (L_d) is the same all along the tape.

TABLE I
COMPOSITION OF CHOSEN TAPE ARCHITECTURES. THE THICKNESSES OF EACH LAYER ARE GIVEN IN PARENTHESIS

Architecture	Substrate	Silver	Shunt
1	Hastelloy (500 μm)	Surround (0.5 μm)	Tin solder (2 μm) + Hastelloy (500 μm)
2	Hastelloy (100 μm)	Surround (1 μm)	Tin solder (10 μm) + Hastelloy (500 μm) + Surround Steelcast (300 μm)
3	Sapphire (3000 μm)	Top of GBCO only (8 μm)	Y_2O_3 (500 μm)

In the FASTGRID project, a value of $E_{max} = 150$ V/m is targeted. The resistance R_L is determined by the nominal current I_n, which is set to $0.5I_c$. We thus have

$$R_L = \frac{E_{max} N L_d}{0.5 I_c}. \tag{6}$$

The resistance of the SFCL is determined as follows. First, the mean conductivity of the tape in the quenched region is calculated using the following expression:

$$\langle \sigma \rangle = \sum_i \frac{\sigma_i t_i}{\sum_i t_i}, \tag{7}$$

where σ_i and t_i are the conductivity and thickness of the ith layer, respectively. The conductivity σ_i of a layer is determined from the average temperature on its cross-section $\langle T_i \rangle$. We assume that the temperature of the whole quenched region is that of the hot spot. This leads to a slight underestimation of the temperature. The error generated by this assumption was verified to be approximately 3%, 11% and 8% for architectures 1, 2 and 3 respectively (see Table I in Section III) .

The total resistance of the SFCL can thus be expressed as

$$R_s = \frac{L_{nz}}{\langle \sigma \rangle S}, \tag{8}$$

where L_{nz} is the total length of the tape in a quenched state, and S is the total area of the cross-section of the tape, which is given by $S = \sum_i w t_i$, where w is the width of the tape.

The total length of the tape that is quenched L_{nz} is given by $N \min(2tv_{nz}, L_d)$, where t is the time elapsed after the generation of the first normal zone and v_{nz} is the NZPV. The factor of 2 represents the fact that the normal zone propagates in both directions along the length of the tape.

Calculations of the NZPV are detailed in Section IV. As we shall see, v_{nz} varies with the applied current. In the 1-D electrothermal model, the value of v_{nz} is considered constant during the whole simulation. Its value is fixed at the beginning of the simulation using the value of the prospective fault current

I_f, where $I_f = V(R_f + R_L)/(R_f R_L)$. However, since v_{nz} depends on the current level (see Section IV), this leads to an underestimation of the temperature. We found that our calculations underestimate the temperature by approximately 16% in the worst case, which corresponds to the situation where $v_{nz} \times 50\,\text{ms} \approx L_d$.

Once R_s is known, the total current in the tape is given by $I = V/R_{tot}$. Using the conductivity of each layer σ_i, as well as their respective cross-sections, it is easy to find the current flowing in each layer.

III. HTS Conductor Design

In this work, we targeted potential tape architectures that met our temperature safety criterion for the two extremes cases: clear fault and single hot spot. The temperature safety criterion was chosen to be 425 K. Therefore, we performed numerical calculations in clear fault and single hot spot conditions for various possible architectures and, based on the results, we chose three promising architectures (see Table I).

Regarding the materials used, we explored several combinations. The superconducting material consisted of a 3.3 μm-thick GdBaCuO (or GBCO) layer. For the substrate, two types of material were considered: Hastelloy and sapphire. While Hastelloy is commonly used in the fabrication of 2G HTS CCs, it is only recently that it was reported that cuprate superconductors could be grown on long length (more than 1 meter) sapphire ribbons [1], [13]. For all architectures, we assumed the presence of a silver layer whose thickness was at least 500 nm on the GBCO layer. Finally, we explored several types of shunt such as Hastelloy (soldered with tin), Steelcast (mix of stycast and micron-sized stainless steel particles) [14] and Y_2O_3. The material properties of Hastelloy, tin, sapphire, Y_2O_3 and silver are easily found in COMSOL materials database or in the literature [8], [15], [16]. The thermal properties of GBCO were taken from [17].

Finally, we assumed that the HTS tape was immersed in a subcooled liquid nitrogen bath whose temperature is 65 K. At $T = 65$ K, the I_c of a 3.3 μm-thick and 12 mm wide GdBaCuO layer was set to 1265 A.

To simulate the clear fault scenario, we set $R_f = 0$, meaning that the whole DC voltage is seen across the SCFL terminals. The resulting maximum temperature in the GBCO layer over time is given in Figure 3, while the current in the tape over time is given in Figure 4.

We observe that the temperature reached after 50 ms is 400 K or below, which satisfies our safety temperature criterion of 425 K. We note that the maximum temperature in the clear fault scenario is lower for architecture 3. This is due to the elevation of silver resistivity when temperature increases, in contrary to Hastelloy, whose resistivity is nearly independent of temperature. This is also seen in Figure 4 where the current decreases faster in the case of architecture 3. However, the peak current is much higher in case of architecture 3 ($\approx$4 kA) in comparison with architectures 1 and 2 ($\approx$2.3 kA for architecture 1 and $\approx$2.7 kA for architecture 2).

An example of current sharing between the layers of architecture 1 in the case of a clear fault is presented in Figure 5. We

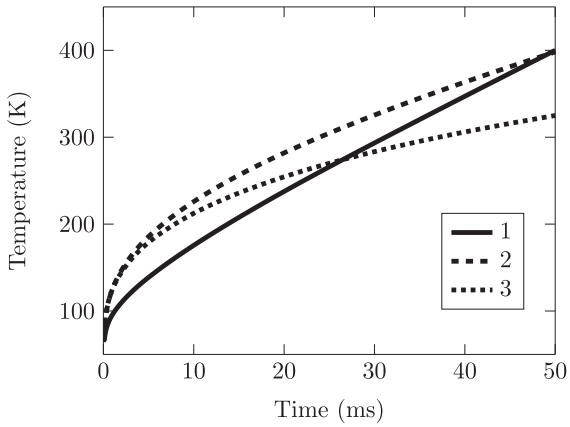

Fig. 3. Maximum temperature calculated in the GBCO layer over time during a clear fault (see Table I for the details of tape architectures 1, 2 and 3).

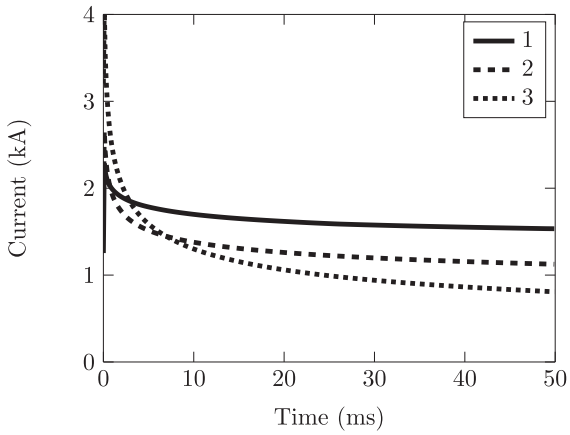

Fig. 4. Total current in the tapes over time during a clear fault.

observe that most of the current flows in the Hastelloy layer since more than 99% of the volume of the tape is made from Hastelloy. We note that the amount of current flowing in the Hastelloy is constant over time, since the electrical conductivity of Hastelloy is almost independent of temperature, while the current in the silver and tin layers diminishes over time.

In the single hot spot scenario, we assumed that the fault current amplitude was equal to I_c (1265 A) and was constant over time, which corresponds to the worst case scenario. The maximum temperatures over time for all architectures are presented in Figure 6. We observe that the maximum temperature is lower than our safety temperature criterion (425 K) for all architectures. We also note that the maximum temperature of architecture 1 after 50 ms is much lower than that of architectures 2 and 3. This can be explained by the lower resistance per meter of architecture 1.

IV. Evaluation of the NZPV

In order to obtain the NZPV of each tape architecture, three-dimensional finite element simulations were run in the Joule heating module of the COMSOL Multiphysics 4.3b software package. Details of the model can be found in Refs. [8], [10].

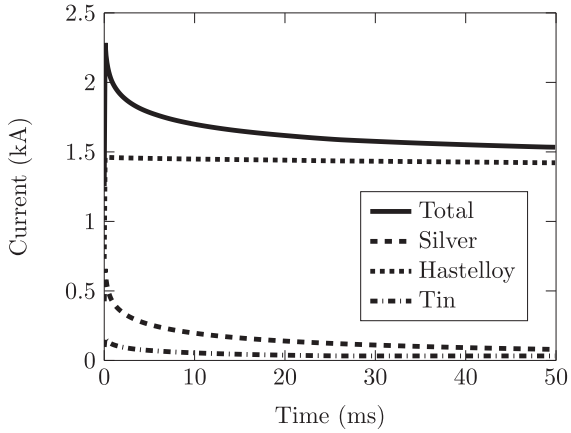

Fig. 5. Example of current sharing between layers of architecture #1 in the case of a clear fault.

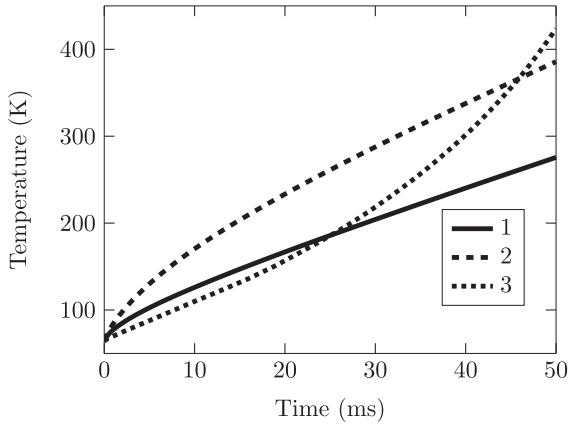

Fig. 6. Maximum temperature calculated in the GBCO layer over time in presence of a single hot spot. The applied current is constant over time and is equal to the critical current (1265 A).

The variables solved for in the model were the electrical potential V and the temperature T. They were calculated using the current continuity equation and heat equation, respectively. The current $I(t)$ was imposed at one end of the tape while the other end was grounded.

The electrical conductivity of GBCO in the flux creep and flux flow regimes was approximated by a power-law model, and the transition from the superconducting state to the normal state was modeled assuming two resistances in parallel. Explicitly, the equations used in the model for the electrical properties of GBCO in the superconducting state were

$$\sigma_{GBCO}(T) = \sigma_{sc}(T) + \sigma_n(T), \tag{9}$$

$$\sigma_{sc}(T) = \frac{J_c(T)}{E_0}\left(\frac{\|E\|}{E_0}\right)^{\frac{1-n(T)}{n(T)}}, \tag{10}$$

where $\sigma_{sc}(T)$ is the conductivity in the superconducting state, $\sigma_n(T)$ is the conductivity in the normal state, $J_c(T)$ is the critical current density, $\|E\|$ is the norm of the electric field, E_0 is the electric field criterion (10^{-4} V/m) and $n(T)$ is a fitting parameter.

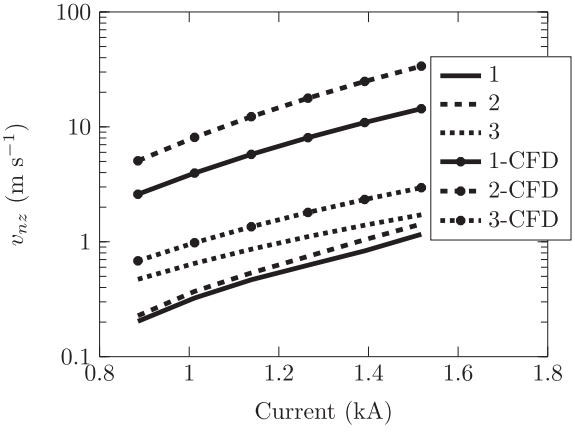

Fig. 7. Dependence of the NZPV with the applied current for all three architectures with and without a CFD.

The critical current density J_c (A/m^2) and n-factor of GBCO in self-field have been obtained experimentally over a temperature range from 25 K up to 90 K by THEVA. They were fitted with polynomial functions. The polynomial functions included in the model were:

$$J_c(T) = 1.54 \times 10^8 \left(4.016 \times 10^{-5}\, T^4 - 8.9 \times 10^{-3}\, T^3 + 7.256 \times 10^{-1}\, T^2 - 35.7T + 1189\right), \tag{11}$$

$$n(T) = 2.99 \times 10^{-7}\, T^5 + 7.546 \times 10^{-5}\, T^4 - 7.844 \times 10^{-3}\, T^3 + 4.259 \times 10^{-1}\, T^2 - 12.12T + 183.4. \tag{12}$$

The dependence of the NZPV with the applied current for each architecture investigated is presented in Figure 7. The values of the NZPV without CFD vary from 0.2 m/s to 1.7 m/s, depending on the applied current. We note that architecture 3 possesses a higher NZPV thanks to its sapphire substrate.

Simulations were also realized for the case where a CFD consisting of a resistive layer covering 90% of the GBCO/Ag interface was inserted in the tape. In the case of architectures 1 and 2, the addition of a CFD increases the NZPV by more than one order of magnitude and NZPVs of more than 30 m/s are predicted. In the case of architecture 3, the gain due to the addition of a CFD is less important and corresponds to a gain factor of approximately 1.5.

V. DC Current Limitation

In Figure 8, we present the maximum temperature over time calculated with the 1-D model for each of the three tape architectures (without CFD) in the case where the prospective fault current equals the critical current and hot spots are generated every meter ($L_d = 1$ m). Comparing with the case of a single hot spot (Figure 6), we observe that the temperatures reached after 50 ms are slightly lower in the case of architectures 1 and 2. In the case of architecture 3, the difference is larger (≈100 K). The reason is due to the higher NZPV of architecture 3 in comparison with architectures 1 and 2 (see Figure 7). The corresponding

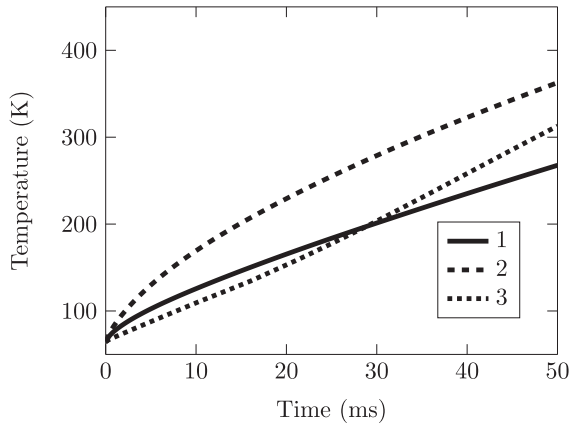

Fig. 8. Maximum temperature calculated in the GBCO layer over time in presence of hot spots located every meter ($L_d = 1$ m) (without CFD). The prospective fault current is equal to the critical current. The NZPV values used in the simulations were 0.61 m/s, 0.75 m/s and 1.1 m/s for architectures 1, 2 and 3 respectively.

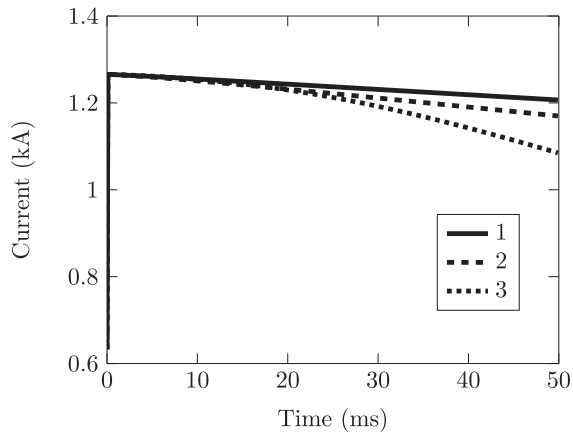

Fig. 9. Limited current over time in presence of hot spots located every meter ($L_d = 1$ m) (without CFD). The prospective fault current is equal to the critical current. The NZPV values used in the simulations were 0.61 m/s, 0.75 m/s and 1.1 m/s for architectures 1, 2 and 3 respectively.

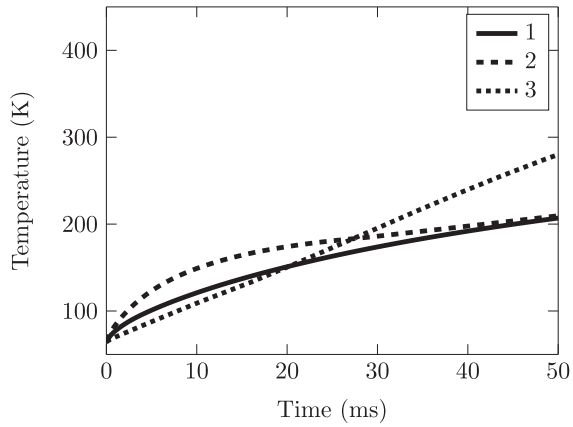

Fig. 10. Maximum temperature calculated in the GBCO layer over time in presence of hot spots located every meter ($L_d = 1$ m) in presence of a CFD. The prospective fault current is equal to the critical current. The NZPV values used in the simulations were 8.06 m/s, 17.78 m/s and 1.8 m/s for architectures 1, 2 and 3 respectively.

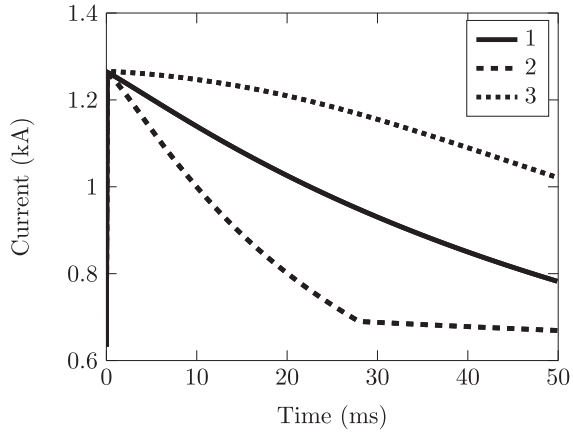

Fig. 11. Limited current over time in presence of hot spots located every meter ($L_d = 1$ m) in presence of a CFD. The prospective fault current is equal to the critical current. The NZPV values used in the simulations were 8.06 m/s, 17.78 m/s and 1.8 m/s for architectures 1, 2 and 3 respectively.

limited current is presented in Figure 9. While the current limitation is rather small for architectures 1 and 2, architecture 3 is more efficient to limit the current due to its higher NZPV. We note also that, for all three architectures, the quench is only partial since the current is still decreasing after 50 ms.

We have seen before (Figure 7) that the insertion of a CFD in a HTS tape can drastically increase the NZPV. In Figure 10, the maximum temperature in the GBCO layer over time is presented for the same parameters as those used for generating Figure 8, except for the NZPV, which was calculated considering the presence of a CFD. We first observe that the temperature reached after 50 ms is lower than in Fig. 8 for all three architectures when a CFD is included. Furthermore, in Figure 11, we observe that the current limitation is more efficient in presence of a CFD. This higher effectiveness is a consequence of the higher NZPV induced by the CFD. For example, in the case of architecture 2, the tape becomes fully quenched at $t \approx 28$ ms (dashed line in Figure 11) and the current corresponds to $\approx$55% of the prospective fault current. This is clearly seen by the change of slope in the variation of the current with time. When no CFD is present in architecture 2 (Figure 9), the limitation of the current is much less effective (the current after 50 ms corresponds to $\approx$93% of the prospective current). This explains why the temperature is much higher in this case after 50 ms: 363 K (without CFD) versus 210 K (with CFD). Regarding architecture 1, similar trends are observed despite the fact that the current limitation is a bit less effective than with architecture 2. In the case of architecture 3 (sapphire substrate), adding a CFD provides benefits, but to a lesser extend. Indeed, as discussed earlier, in the case of architecture 3, the gain in NZPV due to the insertion of a CFD is less important.

We now investigate the effect of the hot spot interdistance. Basically, in our model, when the hot spot interdistance is lower, it corresponds to a higher density of hot spots. In reality, the hot spot interdistance is correlated to the applied current, i.e. $L_d(I)$, and the relationship between L_d and I depends on the distribution of I_c along the length of the tape. Indeed, as the current increases, more and more regions of a HTS tape will

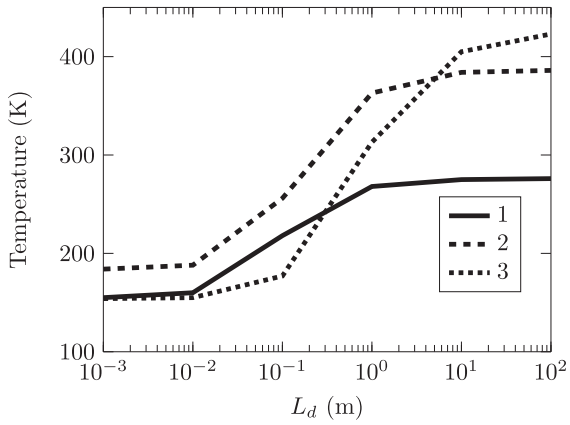

Fig. 12. Maximum temperature calculated in the GBCO layer in presence of hot spots at $t = 50$ ms for various L_d (without CFD). The prospective fault current is equal to the critical current. The NZPV values used in the simulations were 0.61 m/s, 0.75 m/s and 1.1 m/s for architectures 1, 2 and 3 respectively.

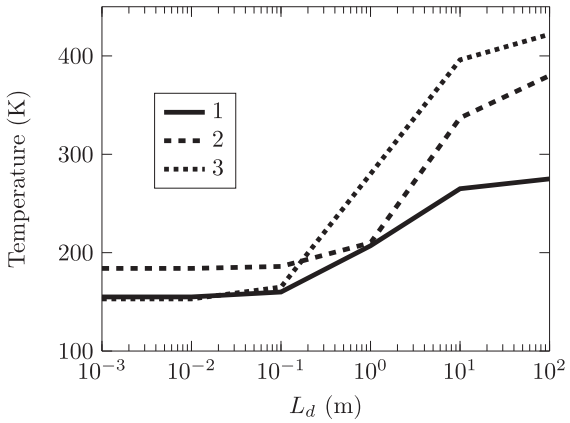

Fig. 13. Maximum temperature calculated in the GBCO layer in presence of hot spots at $t = 50$ ms for various L_d in presence of a CFD. The prospective fault current is equal to the critical current. The NZPV values used in the simulations were 8.06 m/s, 17.78 m/s and 1.8 m/s for architectures 1, 2 and 3 respectively.

quench. However, quantitative values of L_d requires knowing the local I_c along the whole length of the tape, which would require a fine discretization of the tape along its length and would drastically increase computation time.

In Figure 12, the temperature of a hot spot is given versus the hot spots interdistance when the prospective fault current is equal to the critical current. We observe that the temperature is lower when the hot spot interdistance is small (less than 1 cm). The reason is that the tape becomes fully quenched within a period of less than 50 ms, i.e. $v_{nz} L_d < 50$ ms. If the hot spot interdistance is between 1 cm and 1 m, the hot spot temperature increases. The reason is that the NZPV is not high enough to fully quench the tape. Finally, we observe that the temperature of a hot spot is much higher as the density of hot spots becomes lower ($L_d >$10 m) and temperatures similar to the single hot spot case are found (see Figure 6).

When a CFD is integrated in the tape architecture (Figure 13), we observe that the gain in NZPV allows reducing considerably the temperature elevation for a low hot spot density, which reduces the probability of damaging the tape. However, we observe that the temperature reached after 50 ms for $L_d > 10$ m is very close again to the temperature obtained for the single hot spot case.

VI. Concluding Remarks

In this work, we compared various promising tape architectures for HVDC limitation. Firstly, two extreme cases of faults, i.e. clear fault and a single hot spot, were used to design tape architectures whose temperature must remain below a given temperature threshold criterion in all cases. Different substrates and combination of shunts were considered. While a shunt with high heat capacity and high electrical resistance is preferable in the clear fault scenario, the electrical resistance cannot be too high in order to limit the temperature elevation in the single hot spot scenario. A compromise must then be found to survive the quench in both cases. DC limitation experiments will be realized within the FASTGRID project and compared with our numerical calculations.

Our results indicate that the tape architectures investigated in this work are sufficiently robust to survive to any type of fault. However, it would be relevant to reduce the thickness of the metallic layers. This would increase the resistance per unit length, which would reduce the length of HTS tape required in the SFCL. Ultimately, this would translate into lower fabrication costs and a smaller device. If one could design a tape architecture with a NZPV of more than 10 km/s, then this would ensure that the tape is fully quenched even in the worst case scenario of a single hot spot in regards with the FASTGRID requirements. This would also translate in a lower temperature at the hot spot locations and a reduction of the thickness of the metallic layers could really be envisioned.

Eventually, it would be important to develop a more realistic physical model that would allow solving for V and T in 2D (or even 3D), and that would include a real distribution of I_c in a power system analysis software such as EMTP-RV. Efforts in this direction have been made by Bonnard *et al.* [18]. However, the model developed by Bonnard *et al.* could not include a real distribution of I_c due to meshing constraints. Indeed, the size of the elements at the boundary of the normal zone and the superconducting zone must be sufficiently small to represent correctly the physical phenomena. Thus, if one wants to simulate hot spots that can be generated anywhere in the tape with a realistic I_c distribution along the length of the tape, a very fine mesh must be used everywhere in the tape geometry. However, such a fine mesh over long lengths of tape would required an enormous computation time. One possibility would be to use adaptive mesh refinement methods to reduce it.

Finally, an aspect that was not discussed in this work is the dynamics of the generation of hot spot. It is expected that the generation of hot spot will be harder for tapes grown on sapphire simply because of its quite high thermal conductivity. This is an aspect that should be taken in consideration in future work.

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REFERENCES

[1] FASTGRID project. Apr. 25, 2019. [Online]. Available: https://www.fastgrid-h2020.eu

[2] G. Escamez, J. Vialle, C. Bruzek, V. Groe, M. Bauer, and P. Tixador, "Numerical investigations of ReBCO conductors with high limitation electric field for HVDC SFCL," *IEEE Trans. Appl. Supercond.*, vol. 28, no. 4, Jun. 2018, Art. no. 5602705.

[3] A. Badel, G. Escamez, and P. Tixador, "REBCO FCL modelling: Influence of local critical current non-uniformities on overall behavior for various tape architectures," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 3, Jun. 2015, Art. no. 5600504.

[4] G. Celentano *et al.*, "Hot spot stimulated transition in YBCO coated conductors: Experiments and simulations," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 2486–2489, Jun. 2009.

[5] W. K. Chan and J. Schwartz, "Three-dimensional micrometer-scale modeling of quenching in high-aspect-ratio coated conductor tapes part II: Influence of geometric and material properties and implications for conductor engineering and magnet design," *IEEE Trans. Appl. Supercond.*, vol. 21, no. 6, pp. 3628–3634, Dec. 2011.

[6] X. Wang, U. P. Trociewitz, and J. Schwartz, "Self-field quench behaviour of $YBa_2Cu_3O_7$ coated conductors with different stabilizers," *Supercond. Sci. Technol.*, vol. 22, no. 8, 2009, Art. no. 085005.

[7] D. Colangelo and B. Dutoit, "Analysis of the influence of the normal zone propagation velocity on the design of resistive fault current limiters," *Supercond. Sci. Technol.*, vol. 27, no. 12, 2014, Art. no. 124005.

[8] C. Lacroix and F. Sirois, "Concept of a current flow diverter for accelerating the normal zone propagation velocity in 2G HTS coated conductors," *Supercond. Sci. Technol.*, vol. 27, 2014, Art. no. 035003.

[9] C. Lacroix, Y. Lapierre, J. Coulombe, and F. Sirois, "High normal zone propagation velocity in second generation high-temperature superconductor coated conductors with a current flow diverter architecture," *Supercond. Sci. Technol.*, vol. 27, 2014, Art. no. 055013.

[10] C. Lacroix, F. Sirois, and J-H. Fournier Lupien, "Engineering of second generation HTS coated conductor architecture to enhance the normal zone propagation velocity in various operating conditions," *Supercond. Sci. Technol.*, vol. 30, no. 6, 2017, Art. no. 064004.

[11] F. Roy, M. Therasse, B. Dutoit, F. Sirois, L. Antognazza, and M. Decroux, "Numerical studies of the quench propagation in coated conductors for fault current limiters," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 2496–2499, Jun. 2009.

[12] L. Antognazza *et al.*, "Comparison between the behavior of HTS thin film grown on sapphire and coated conductors for fault current limiter applications," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 1960–1963, Jun. 2009.

[13] A. Saraf, B. Almog, M. Azoulay, and G. Deutscher, "Sapphire-based SFCL conductors," in *Superconducting Fault Current Limiter*, P. Tixador, Ed., Singapore: World Scientific Publishing Co. Pte. Ldt., 2019, ch. 17, pp. 357–372.

[14] E. J. Wollack, D. J. Fixsen, R. Henry, A. Kogut, M. Limon, and P. Mirel, "Electromagnetic and thermal properties of a conductively loaded epoxy," *Int. J. Infrared Millimeter Waves*, vol. 29, no. 1, pp. 51–61, Jan. 2008.

[15] *COMSOL Multiphysics. 4.3b*. Stockholm, Sweden: COMSOL AB. [Online]. Available: www.comsol.com

[16] F. Roy, "Modeling and characterization of coated conductors applied to the design of superconducting fault current limiters," Ph.D. dissertation, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, 2010.

[17] H. Fujishiro, K. Katagiri, A. Murakami, Y. Yoshino, and K. Noto, "Database for thermal and mechanical properties of REBaCuO bulks," *Physica C Supercond.*, vol. 426–431, pp. 699–704, 2005.

[18] C.-H. Bonnard, F. Sirois, C. Lacroix, and G. Didier, "Multi-scale model of resistive-type superconducting fault current limiters based on 2G HTS coated conductors," *Supercond. Sci. Technol.*, vol. 30, no. 1, 2017, Art. no. 014005.